Gigachip Timing Closure in FinFET Process Node

Dorado Design Automation, Inc.

ABSTRACT

TSMC FinFET technology is the right answer for better PPA, but it also means a lot more challenge at chip implementation, as the new technology enables integration of more functions into a chip even it is a power sensitive design. Nevertheless, at ECO phase we are seeing a growing number of supper size of hierarchical designs. For example, if we are doing Timing ECO for a huge hierarchical chip, we would expect very fast timing closure in top design integration; but if we are working on a bottom level of timing closure, we would like to get the best accurate timing to do boundary optimization to reach the best timing performance. The traditional way of timing closure no longer satisfies the needs of tackling these increasing and various types of challenge.

In this presentation, attendees will see several ECO strategies for timing closure in advanced process node of gigachip design, such as:

Hierarchical ECO Flow: fast timing closure of huge hierarchical design.

Advanced ECO Solution: efficiently address timing critical paths and well optimized boundary timing paths.

Wire ECO Solution: minimum wire delay to shorten timing closure cycle time.

In addition to the specific ECO flows for specific cases, Dorado's latest Tweaker ECO Platform is N10/N7 color rule compliant and aware of pin access rules so it can hand off a legalized routable db to P&R tools.

Dorado and TSMC have partnered in making the innovative and practical ECO flows. While moving forward to N10/N7 technology, there are more challenge we are facing during ECO cycle. In fact, it is another successful story happen at Open Innovation Platform.

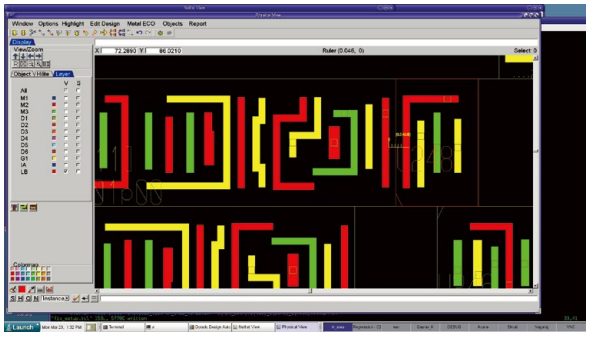
Gigachip Timing Closure in FinFET Process Node

Kenneth Hung, Technical Consulting Manager
Dorado Design Automation, Inc.

TSMC OIP Innovation Platform Ecosystem Forum 2016

Process Trends and Challenges

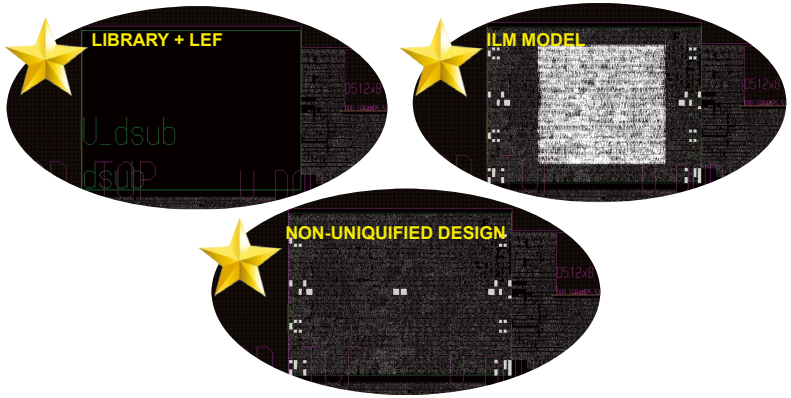
- FinFET rules aware
  - 20nm process : MIN. VT WIDTH / SPACING/AREA RULEs.
  - 16nm process : HORIZONTAK ABUTMENT / DPT RULEs.
  - 10nm process : TPO WIDTH / SPACING/COLORING RULEs.
  - 7nm process : VERTICAL ABUTMENT / ROUTABILITY RULEs.



Design Trends and Challenges

Mutual Cus

- Hierarchical design aware
  - TYPE1 : SUB-DESIGN MODELED BY LIB/LEF.
  - TYPE2 : SUB-DESIGN BY ILM MODEL.
  - TYPE3 : UNIQUIFIED/NON-UNIQUIFIED SUB-DESIGNS.

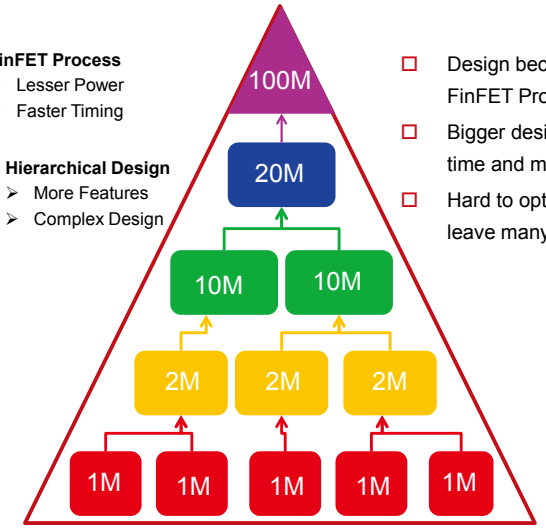


Challenge in Gigachip FinFET Design

FinFET Process
- Lesser Power
- Faster Timing

Hierarchical Design
- More Features
- Complex Design

Mutual Customers

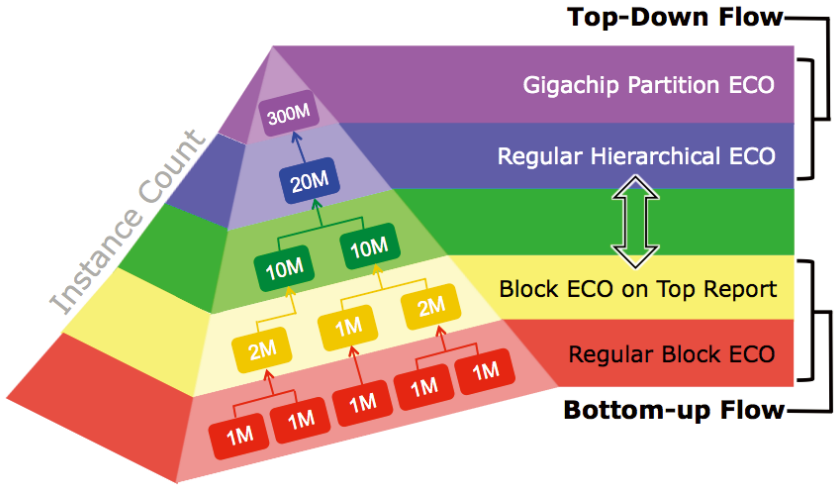


- Design become more complex : FinFET Process + Hierarchical Design
- Bigger design introduce longer run time and more iteration during ECO.
- Hard to optimize entire design and leave many sweet spots in between.

Note: Unit = Instance count

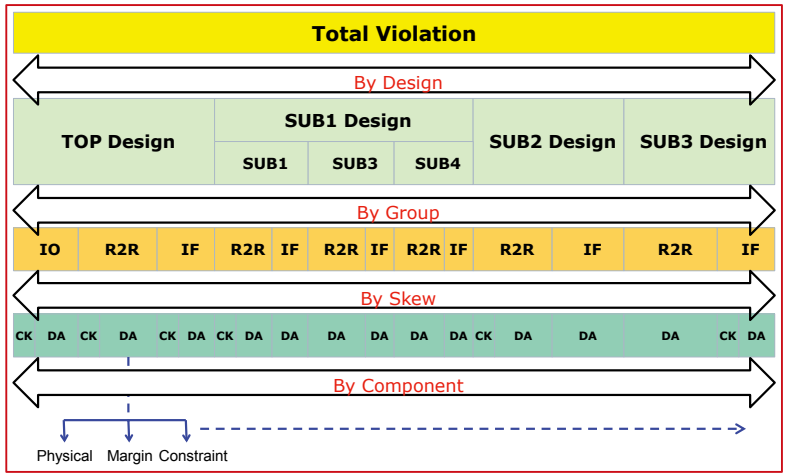
Gigachip ECO Flow

New ECO Solution in Gigachip FinFET Design



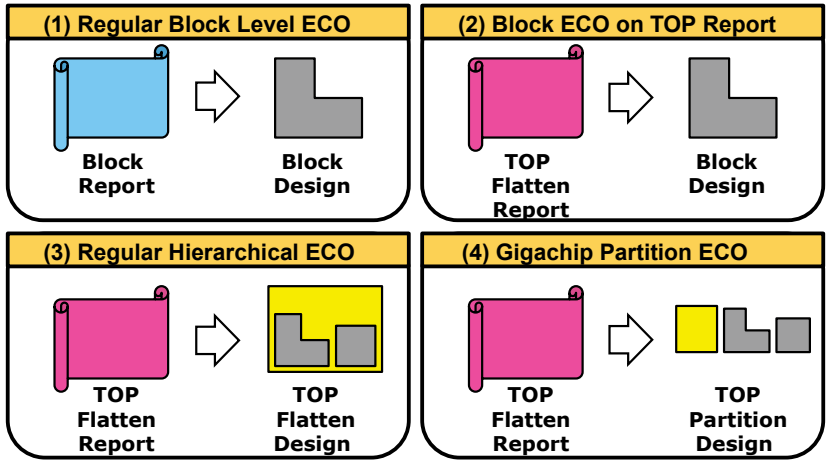
Strategies for Various Challenges (1/4)

- Analysis violation through hierarchical design



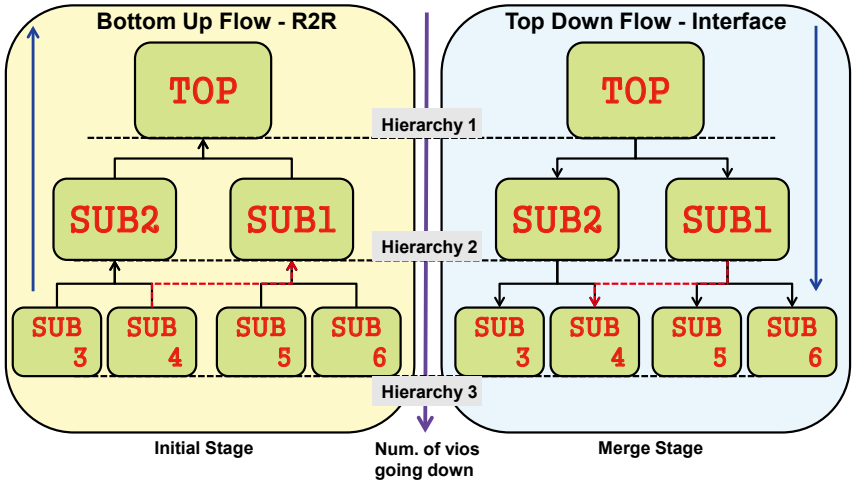
Strategies for Various Challenges (2/4)

- Decide ECO methodology



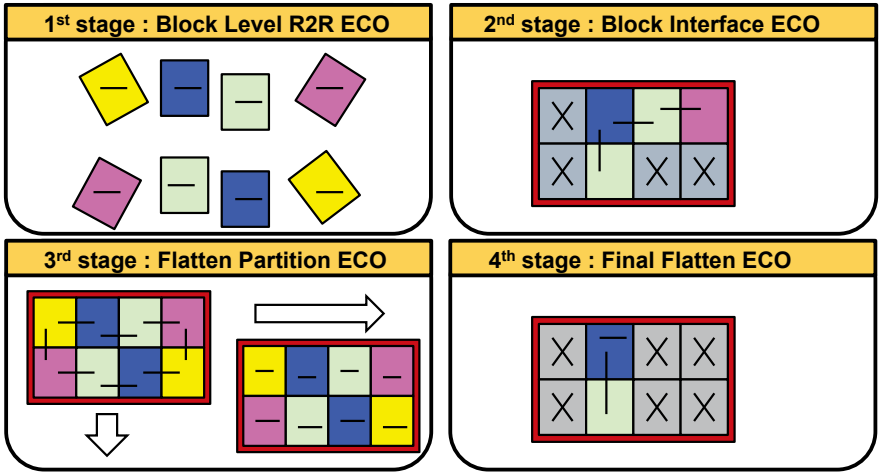
Strategies for Various Challenges (3/4)

- Select ECO flow



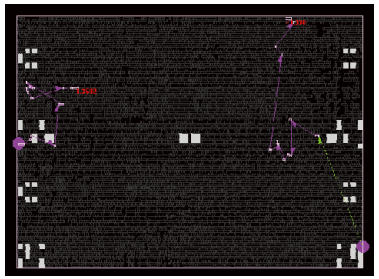
Strategies for Various Challenges (4/4)

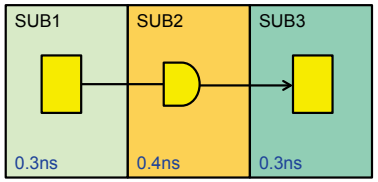
- Decide ECO timing



Slack Budgeting in Hierarchical ECO Flow

- For setup ECO
  - Partition the slack into each ECO block

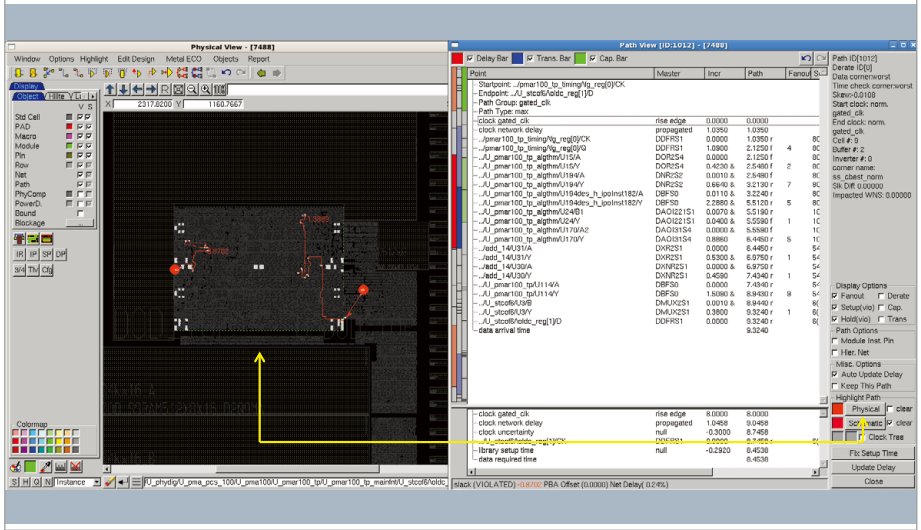




setup slack value -0.5ns
Path length 1ns (0.3+0.4+0.3)

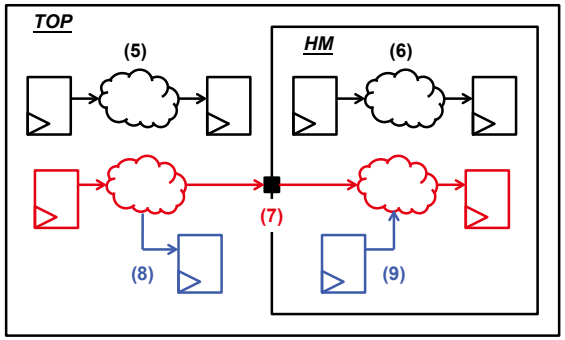
slack value -0.5 x (0.3/1)	slack value -0.5 x (0.4/1)	slack value -0.5 x (0.3/1)
New slack = -0.15ns	New slack = -0.2ns	New slack = -0.15ns

TWEAKER "Path Filters" : R2R, IO, Interface

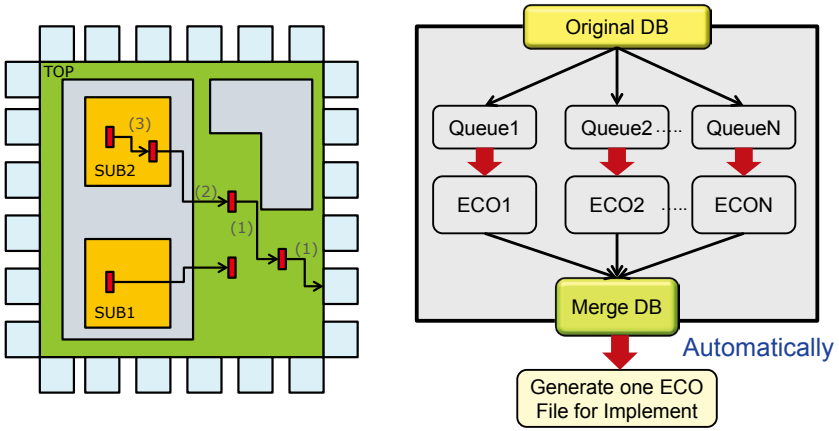


Path Filters : R2R & Interface

- Violation partition



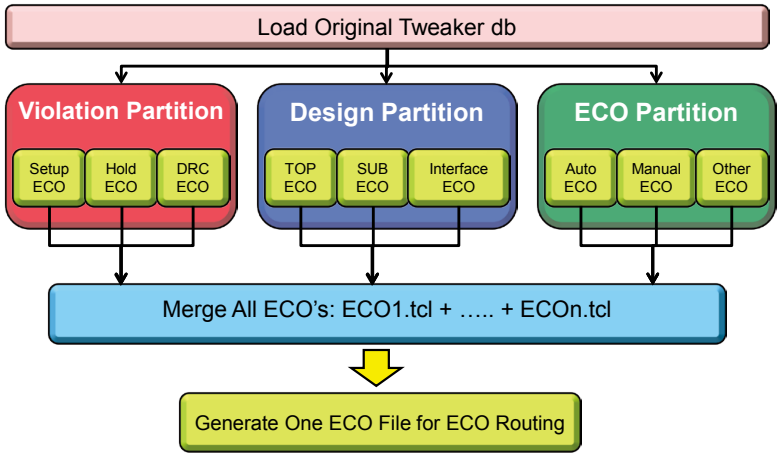
Basic Auto-Partition Flow



More partition, more run time reduction !

Advanced ECO Partition Flow

- The more partitions, the more run time and memory saving !



Gigachip Partition Case 1

Setup (new)	Sizing count	Insert count	Remain vios	Run time
Part1 : top R	19430	18	19139(19094)	01:30:00
Part2 : part1R	371	0	19142(18861)	00:24:00
Part3 : part2R	40024	227	19086(4878)	03:30:00
Part4 : Interface	29281	1045	17986(15012)	03:29:00
Total	89106	1290	19098(1708)	03:30:00
Regular Hier. ECO	87773	608	17857(1619)	10:05:00

- TSMC 16nm Design (18 scenarios)
- Hierarchical Design : 13M instances (1 TOP + 6HM)
- Hierarchical partition flow has close timing result and saves 6.5 hrs of run time.

Gigachip Partition Case 2

Power eco	VT swap 10	Sizing	Leakage (mW)	Run time
TOP: top R	1408292	642575	5.6%	03:27:39
Part1 : HM 2 R	441478	187259	0.9%	02:46:54
Part2 : HM 2 R	823258	527759	4.5%	04:32:35
Part3 : HM 2 R	250769	90359	0.1%	01:22:29
Part4 : HM 2 R	396243	229977	1.1%	02:33:23
Part5 : interface	359097	324622	3.5%	03:11:57
Total	3679137	2002551	15.6%	04:32:35
Regular	3783650	2090723	15%	13:35:45

- TSMC 16nm Design (3 scenarios)
- Hierarchical Design : 15M instances (1 TOP + 9HM)
- Hierarchical partition flow has close leakage result and saves 9hrs of run time.

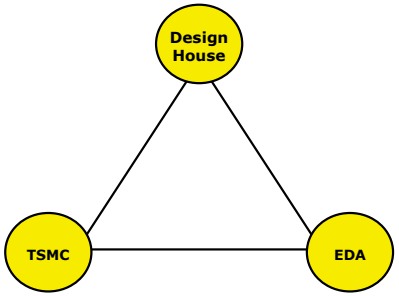
Quick Look of Tweaker-T1 Major Features

Features	Descriptions
Fix Setup	Swap / Size / **Bypass** / **Split Load** / **Pin Swap** / **Move** / **Split Cell**…etc.
Fix Hold	Swap / Size / **Dummy Load** / **HFI** / Insert Delay / **Inv Pair**…etc.
Fix Max. Trans / Cap / Glitch	Swap / Size / **HFS** / **Inv Pair**
Leakage Power Opt.	Swap / Size / **Remove Buf** / **Remove Inv**
Dynamic Power Opt.	**Swap** / **Size** / **Remove Buf** / **Remove Inv**
Skew-Tuning	**Swap** / **Size** / **Dummy Load** / **Insert Buf**
Metal ECO Flow	**Spare Cells + Gate Array + ECO Filler**
ECO Place	**Place Functional ECO Cells for Timing Check & Fix**
HackSDF	**For Early PostSim**
Bus Balance	**SI / Long / Short Paths Optimization**
Area Recovery	**Remove Buf / Inv-pair / Sizing**
Routing Recovery	**Collect Detour / SI / Jog / Low-level Nets / Congestion Aware**
Support Hierarchical Design	Whole Chip / ILM / ETM / Hyper Scale
Support APR ECO tcl	**ICC / ICC2 / SOCE / Innovus / Atop / Olympus**
Support STA Sign-off Tool	**PT / Tempus / ETS / GT / TC / PFX**

Note: Tweaker Only Feature

Keynotes for Gigachip Timing Closure in FinFET Design

- **ECO challenges are ever-increasing with advanced designs**
  - Design become more complex due to FinFET Process + Hierarchical Design
- **Key Enhancements**
  - Regular Block Level ECO
  - Block ECO on Top Report
  - Regular Hierarchical ECO
  - Gigachip Partition ECO



Great Team, Great Collaboration!!

Dorado

Your Virtual CAD Team for All ECO Solutions

www.dorado-da.com